

**CLAIMS**

What is claimed is:

5 1. An on-chip inductor consisting of:

at least one dielectric layer;

10 at least one conductive winding on the at least one  
dielectric layer; and

P-well having a major surface parallel to a major surface  
of the dielectric layer.

15 2. The on-chip inductor of claim 1 further consists of:

a field oxide having a major surface that is juxtaposed to  
the major surface of the P-well.

20 3. The on-chip inductor of claim 1 further consists of:

the at least one dielectric layer including one layer; and

25 the at least one conductive winding including a spiral  
winding on the one layer.

4. The on-chip inductor of claim 1 further consists of:

30 the at least one dielectric layer includes a plurality of  
layers; and

the at least conductive winding includes a plurality of windings on the plurality of layers.

5. The on-chip inductor of claim 1 further consists of:

the at least one dielectric layer includes a plurality of layers; and

10 the at least conductive winding includes a plurality of spiral windings on the plurality of layers.

6. The on-chip inductor of claim 1 further consists of:

15 a substrate having a major surface parallel to the major surface of the at least one dielectric layer.

7. The on-chip inductor of claim 1 further consists of:

20 a secondary winding magnetically coupled to the conductive winding.

8. The on-chip inductor of claim 1, wherein the at least one conductive winding further consists of:

25 center tap operably coupled to a reference potential to produce a differential inductor.

9. An on-chip inductor consisting of:

at least one dielectric layer;

5 at least one conductive winding on the at least one dielectric layer; and

field oxide layer having a major surface parallel to a major surface of the dielectric layer.

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10. The on-chip inductor of claim 9 further consists of:

P-well having a major surface that is juxtaposed to the major surface of the field oxide layer.

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11. The on-chip inductor of claim 9 further consists of:

a secondary winding magnetically coupled to the conductive winding.

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12. The on-chip inductor of claim 9, wherein the at least one conductive winding further consists of:

25 center tap operably coupled to a reference potential to produce a differential inductor.

13. An on-chip inductor consisting of:

at least one dielectric layer;

5 at least one conductive winding on the at least one dielectric layer; and

poly silicon layer having a major surface parallel to a major surface of the dielectric layer.

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14. The on-chip inductor of claim 13 further consists of:

a secondary winding magnetically coupled to the conductive winding.

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15. The on-chip inductor of claim 13, wherein the at least one conductive winding further consists of:

center tap operably coupled to a reference potential to

20 produce a differential inductor.

16. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

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creating at least one conductive winding on the at least one dielectric layer; and

10 creating a P-well having a major surface parallel to a major surface of the dielectric layer.

17. The method of claim 16 further consists of:

creating a field oxide having a major surface that is

15 juxtaposed to the major surface of the P-well.

18. The method of claim 16 further consists of:

creating the at least one dielectric layer to include one 20 layer; and

creating the at least one conductive winding to include a spiral winding on the one layer.

25 19. The method of claim 16 further consists of:

creating the at least one dielectric layer to include a plurality of layers; and

30 creating the at least conductive winding to include a plurality of single windings one the plurality of layers.

20. The method of claim 16 further consists of:

creating the at least one dielectric layer to include a plurality of layers; and

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creating the at least conductive winding to include a plurality of spiral windings one the plurality of layers.

21. The method of claim 16 further consists of:

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creating a substrate having a major surface parallel to the major surface of the at least one dielectric layer.

22. The method of claim 16 further consists of:

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creating a secondary winding magnetically coupled to the conductive winding.

23. The method of claim 16, wherein the at least one conductive winding further consists of:

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creating a center tap operably coupled to a reference potential to produce a differential inductor.

24. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

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creating at least one conductive winding on the at least one dielectric layer; and

10 creating a field oxide layer having a major surface parallel to a major surface of the dielectric layer.

25. The method of claim 24 further consists of:

15 creating a P-well having a major surface that is juxtaposed to the major surface of the field oxide layer.

26. The method of claim 24 further consists of:

20 creating a secondary winding magnetically coupled to the conductive winding.

27. The method of claim 24, wherein the at least one conductive winding further consists of:

25 creating a center tap operably coupled to a reference potential to produce a differential inductor.

28. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

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creating at least one conductive winding on the at least one dielectric layer; and

10 creating poly silicon layer having a major surface parallel to a major surface of the dielectric layer.

29. The method of claim 28 further consists of:

15 creating a secondary winding magnetically coupled to the conductive winding.

30. The method of claim 28, wherein the at least one conductive winding further consists of:

20 creating a center tap operably coupled to a reference potential to produce a differential inductor.